CREATING OPTIMIZED PHYSICAL IMPLEMENTATIONS FROM HIGH-LEVEL DESCRIPTIONS OF ELECTRONIC DESIGN USING PLACEMENT-BASED INFORMATION

Abstract of the Disclosure

[0133] An electronic design automation system provides optimization of RTL models of electronic designs, to produce detailed constraints and data precisely defining the requirements for the back-end flows leading to design fabrication. The system takes a RTL model of an electronic design and maps it into an efficient, high level hierarchical representation of the hardware implementation of the design. Automatic partitioning partitions the hardware representation into functional partitions, and creates a fully characterized performance envelope for a range of feasible implementations for each of the partitions, using accurate placement based wire load models. Chip-level optimization selects and refines physical implementations of the partitions to produce compacted, globally routed floorplans. Chip-level optimization iteratively invokes re-partitioning passes to refine the partitions and to recompute the feasible implementations. In this fashion, a multiple-pass process converges on an optimal selection of physical implementations for all partitions for the entire chip that meet minimum timing requirements and other design goals. The system outputs specific control and data files which thoroughly define the implementation details of the design through the entire back-end flow process, thereby guaranteeing that the fabricated design meets all design goals without costly and time consuming design iterations.